AMENDMENTS TO THE CLAIMS

Claim 1. (Previously Presented) A method for determining a control block index for a data cell received by a network processor coupled to an ATM network comprising:

receiving a data cell at a port, the data cell having a virtual path identifier and a virtual channel identifier;

determining a port number for the port;

employing bits of at least one of the virtual path identifier, the virtual channel identifier and the port number to create a first address;

employing the first address to access a first memory and to obtain a first entry from the first memory, the first entry specifying:

a first base memory address;

a number of bits of the port number to use in the control block index; a number of bits of the virtual path identifier to use in the control block index; and

a number of bits of the virtual channel identifier to use in the control block index; and

employing the first base memory address and the number of bits of the port number, virtual path identifier–and virtual channel identifier specified by the first entry to create the control block index for the data cell.

Claim 2. (Original) The method of claim 1 wherein employing bits of at least one of the virtual path identifier, the virtual channel identifier and the port number to create

the first address comprises employing bits of at least one of the virtual path identifier and the port number to create the first address.

Claim 3. (Original) The method of claim 1 wherein the first memory is an on-chip memory of the network processor.

Claim 4. (Original) The method of claim 3 wherein the first memory comprises an on-chip random access memory.

Claim 5. (Original) The method of claim 1 wherein employing the first base memory address and the number of bits of the port number, virtual path identifier and virtual channel identifier specified by the first entry to create the control block index for the data cell comprises:
selecting the number of bits of the port number specified by the first entry;
selecting the number of bits of the virtual path identifier specified by the first entry;
selecting the number of bits of the virtual channel identifier specified by the first entry;
catenating any selected bits; and
adding the catenated selected bits to the first base memory address.

Claim 6. (Original) The method of claim 5 further comprising:
shifting the control block index; and

adding the shifted control block index to a main system memory base offset so as to generate a control block memory address.

Claim 7. (Original) The method of claim 6 further comprising employing the control block memory address to obtain a control block from a main system memory.

Claim 8. (Original) The method of claim 5 further comprising verifying that non-selected port number, virtual path identifier and virtual channel identifier bits are zeroed.

Claim 9. (Original) The method of claim 1 further comprising pre-selecting which bits are used to form the first address.

Claim 10. (Original) The method of claim 1 further comprising selecting each entry for the first memory.

Claim 11. (Currently Amended) A system adapted to determine a control block index for each data cell received by a network processor coupled to an ATM network comprising:
a first memory having a plurality of entries, each entry including:
    a base memory address;
    a number of bits of a port number of a port that receives a data cell to use in the control block index;
    a number of bits of a virtual path identifier of the data cell to use in the control block index; and

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a number of bits of a virtual channel identifier of the data cell to use in the control block index; and a logic circuit adapted to:

generate an address for accessing the first memory based on bits of at least one of a port number of a port that receives a first data cell, a virtual path identifier for the first data cell and a virtual channel identifier for the first data cell;

employ the address to obtain an entry of the first memory; and

employ the base memory address and the number of bits of the port number, virtual path identifier and virtual channel identifier specified by the entry to create a control block index for the first data cell.

Claim 12. (Original) The system of claim 11 wherein the first memory is an on-chip memory of the network processor.

Claim 13. (Original) The system of claim 11 wherein the logic circuit is adapted to create the control block index for the first data cell by:
selecting the number of bits of the port number specified by the entry of the first memory;
selecting the number of bits of the virtual path identifier specified by the entry; selecting the number of bits of the virtual channel identifier specified by the entry;
catenating any selected bits; and
adding the catenated selected bits to the base memory address specified by the entry to form the control block index.

Claim 14. (Original) The system of claim 13 wherein the logic circuit is further adapted to:

shift the control block index; and

add the shifted control block index to a main system memory base offset so as to generate a control block memory address.

Claim 15. (Original) The system of claim 11 further comprising a processor coupled to the first memory and the logic circuit and adapted to:

determine each entry within the first memory; and

determine which bits of a port number of a port that receives a data cell, a virtual path identifier for the data cell and a virtual channel identifier for the data cell are employed to generate an address for the first memory.

Claim 16. (Original) A method for address mapping in a network processor, the method comprising:

determining a port number of a port that receives a data cell;

determining a virtual path identifier and a virtual channel identifier for the data cell;

creating a first index based on at least one of the port number, the virtual path identifier and the virtual channel identifier;

accessing one of a plurality of entries stored in a first on-chip memory using the first index;

creating a second index based on the accessed entry of the first on-chip memory; and

accessing an entry of a second memory based on the second index.

Claim 17. (Original) The method of claim 16 wherein each entry stored in the first on-chip memory contains a base address field and one or more of a number of port number bits field, a number of virtual path identifier bits field and a number of virtual channel identifier bits field.

Claim 18. (Original) A system adapted to perform address mapping in a network processor comprising:
a first on-chip memory having a plurality of entries; and
a logic circuit adapted to:
create a first index based on at least one of a number of a port that receives a data cell, a virtual path identifier for the data cell and a virtual channel identifier for the data cell;
access one of the plurality of entries stored in the first on-chip memory using the first index; and
create a second index based on the accessed entry of the first on-chip memory.

Claim 19. (Original) The system of claim 18 wherein each entry of the first on-chip memory contains a base address field and one or more of a number of port number bits field, a number of virtual path identifier bits field and a number of virtual channel identifier bits field.